

## MC68HC912B32 EEPROM, FLASH MEMORIES AND BDM

MC68HC912B32 /4J54E; 9H91F/ memories could be access with ETL MC68HC912/9S12 FLASH/EEPROM programmer via in-circuit programming interface.

### **FLASH EEPROM**

The MC68HC912B32 version of M68HC12 has 32 kbytes of FLASH EEPROM. This FLASH EEPROM design is similar to standard EEPROM in that it is nonvolatile and can be programmed and erased electrically. It offers the advantages of faster programming and erasing but can be bulk erased only. Also *IT DOES NOT HAVE A CHARGE PUMP*, so an external programming voltage must be supplied.

As fact, FLASH EEPROM cells are smaller than EEPROM cells and can thus provide more storage per unit area. The FLASH EEPROM is configured and can be read as either bytes, aligned words or misaligned words. It can be programmed *ONLY* in byte or aligned words. The initial location for the FLASH EEPROM depends on the operating mode. In single-chip mode memory resides at \$8000-\$FFFF on reset. For the expanded mode FLASH EEPROM is located from \$0000-\$7FFF but is disabled initially and location \$8000-\$FFFF are mapped to be used with external memory.

#### FLASH EEPROM PROGRAMMING VOLTAGE:

### **WARNING**

V<sub>fp</sub> : MUST BE KEPT HIGHER THAN V<sub>dd</sub> – 0.5V AT ALL TIMES OR THE FLASH EEPROM CAN BE DAMAGED. TYPICAL 11.4...12.0V. DEFINED AS MIN. 11.2V

Unlike EEPROM the programming voltage for the FLASH EEPROM must be supplied from an external source. The programming voltage V<sub>fp</sub> is nominally +12 Volts\* (see WARNING). For programming, when the chip in read mode V<sub>fp</sub> must be equal to V<sub>dd</sub> ± 0.35V. You can control this voltage in two ways (see figure 1) requires external circuit.

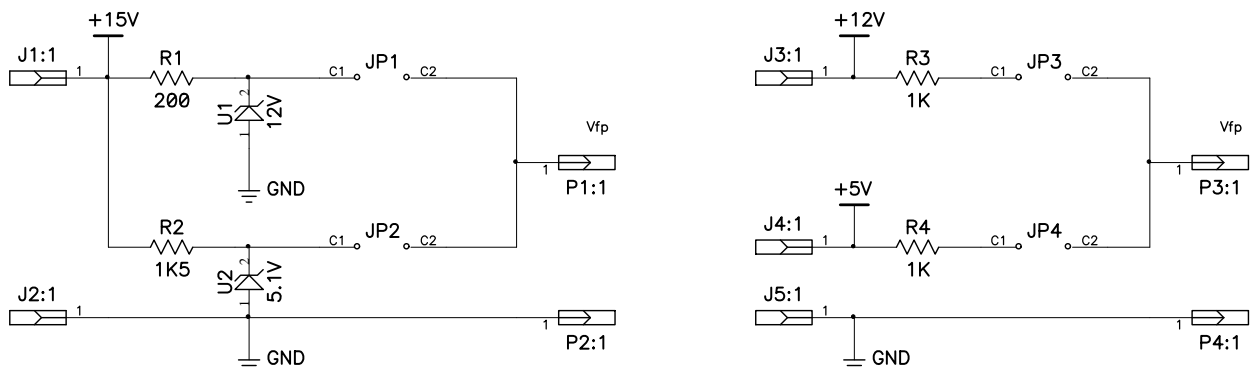


Figure 1.

FLASH EEPROM may be erased and programmed only 10...100 times. The erase time for the FLASH EEPROM is at least a factor of 10 longer than the EEPROM. The data retention, defined as minimum, 10 years. FLAH EEPROM programming characteristics summed in the Table 1:

Measurement	Minimum	Typical	Maximum	Units
Number of programming pulses			50	pulses
Programming pulse width	20		25	microseconds
The time delay after programming	10			microseconds
Programming margin	100			%
Number of erase pulses			5	pulses
Erase pulse width	90	100	110	milliseconds
The time delay after erasing	1			milliseconds
Erase margin	100	100		%
Program/erase endurance	10**	100		Cycles
Data retention	10			Years

Table 1.

\*\* NOTE: 10 cycles for early versions of M68HC12

## EEPROM

The EEPROM can be programmed without an additional power supply, because a charge pump has been include to develop the programming voltage. The initial location in Single-Chip mode for the EEPROM at \$0D00-\$0FFF; 768 bytes. The location of the EEPROM can be remapped to any 4-Kbyte block and the EEPROM can be disabled by writing INITEE register. The EEPROM has a minimum program/erase life of 10000 cycles over its complete operating temperature range.

### EEPROM PROGRAMMING VOLTAGE:

A high voltage (higher than the normal 5V operating voltage) is required to program and erase EEPROM memory. For the M68912, a 19V programming voltage must be supplied. The internal charge pump circuit generate this voltage on the chip without any external source. The system clock is used as an oscillator to pump Vdd up to the 19V required by the EEPROM. If the system clock frequency is less than Fprog (1Mhz) an internal RC oscillator must be turned ON. The Fprog frequency may change in different versions of M68HC912 CPUs.

The EEPROM is organized as a 16-bit memory. The EEPROM can be read as either bytes, aligned words or misaligned words. Aligned words are 16 bits with the most significant byte at an even address. A misaligned word will be 16 bits with the most significant byte at an odd address. For example:

1 – Byte:

LDAA \$1000 ; (\$1000) to A  
LDAA \$1001 ; (\$1001) to A

2 – Aligned word:

LDD \$1000 ; (\$1000) to A (\$1001) to B  
 LDD \$1002 ; (\$1002) to A (\$1003) to B

3 – Misaligned word:

LDD \$1001 ; (\$1001) to A (\$1002) to B

EEPROM programming characteristics summed in the Table 2:

Measurement	Minimum	Typical	Maximum	Units
Min. programming clock frequency	1			MHz
Programming time			10	milliseconds
Clock recovery following stop			10	milliseconds
Erase time			10	milliseconds
Program/erase endurance	10000		30000	Cycles
Data retention	10			Years

Table 2.

Before programming a location in EEPROM, check to see if it can be programmed (all bits in their erased state - \$FF). If not, you must first erase it. EEPROM of MC68HC912B32 can be protected from programming and erasing. The default (reset) state of EEPROM register of each BPROT bit is 1, but in ISP mode D-Bug12 monitor you'll find the bits are reset, allowing you to program the EEPROM without first charging them. The five blocks could be protected in Expanded and Single-Chip modes: \$0FC0-\$0FFF (64 bytes); \$0F80-\$0FBF (64 bytes); \$0F00-\$0F7F (128 bytes); \$0E00-\$0EFF (256 bytes); \$0D00-\$0DFF (128 bytes).

### Background Debug Module (BDM)

The MC68HC12 BDM system uses a single wire plus ground for all debugging. The BDM system in M68HC12 allows access to the internal operation of the target system and does not interfere with the application hardware or software. M68HC12 uses a separate serial I/O interface (BKGD pin) and no user memory. With the M68HC12 BDM you need only provide a way to connect ground, BKGD and reset pins. In fact, in the M68HC12 you can even read or write target system memory locations without stopping the running application program. The M68HC12 also includes logic for tracing a single instruction at a time in the target system. And its name implies, the BDM system is primarily intended for system development and debug, however the BDM system is also useful for other application purposes. It can be used to load/reload an application program into a target system after it has been completely assembled. In a data logging applications, the BDM could be used to retrieve logged data, thus making it unnecessary to add this function to the application software. A typical BDM system consist of a desktop PC, interface pod and the target M68HC12 system. The link from PC to the interface pod is a simple RS232 asynchronous serial port. Motorola has defined a standard six pin connector to allow a pod to be connected to any target M68HC12 system. The connection can be simple as the BKGD, reset and ground pins. Vdd connection allows not use additional power supply source to the target system. A fifth pin could be used to supply an 11.4-12.0V Flash programming voltage to the target system although this pin is usually not used. The BKGD pin is used for three functions in the M68HC12 MCU. During reset, this pin is a mode select input that selects between normal (BKGD = 1) and special (BKGD = 0) modes of operations. After reset this pin becomes the dedicated serial interface pin for the background debug mode. If an appropriate serial command is received, BKGD can be used to tag selected program instructions in the instruction queue. The BDM system is ALWAYS REGARDLESS OF OPERATION MODE.

There are seven BDM registers that are mapped into addresses \$FF00-\$FF06 when BDM is active. Only two of these, the BDM status register at \$FF01 and the BDM CCR Holding Register at \$FF06 are of interest to the program writer. The other registers are for use only by BDM firmware and logic. The typical BDM system shown on Figure 2:

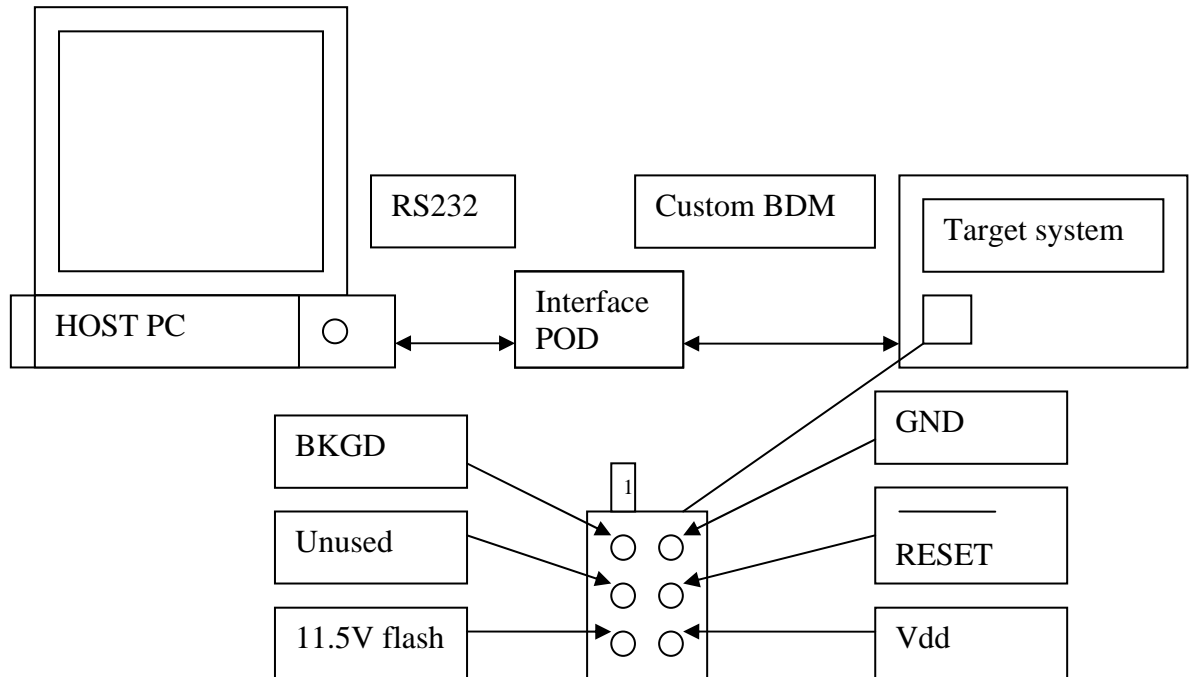


Figure 2.

When the programmer is removed, make sure that the BKGD pin is pulled up through a simple pull-up resistor (nominal 10K) and the target system will reset in normal single-chip mode.